We Claim:

1. A method for increasing security of a CPU containing a pipeline having at least one decode stage and one write back stage, the write back stage having at least one first register whose use does not result in any state change of the CPU, and at least one second register whose use does result in a state change of the CPU, which comprises the steps of:

inserting at least one randomly selected code sequence that does not cause a state change of the CPU in the decode stage as one of a placeholder code and a dummy code sequence; and

selecting the randomly selected code sequence so as to obtain a program execution time that is different from previous program runs on each run of the specific program.

2. The method according to claim 1, which further comprises reading the randomly selected code sequence from a memory using at least one randomly determined memory address.

3. The method according to claim 2, which further comprises using a ROM as used the memory.

4. The method according to claim 1, which further comprises providing the CPU with means for selecting the randomly selected code sequence such that the execution time of the

specific program varies with each program run of the specific program.